REMARKS

The present Amendment is in response to the Office Action having a mailing date of October 23, 2002. Claims 1-20 are pending in the present Application. Claims 1-20 are rejected. Applicant has amended the claims 1, 4, 5, 8 and 15 for clarification. Claims 2 and 3 have been cancelled. Consequently, claims 1 and 4-20 remain pending in the present application.

Drawings

The Examiner states:

Figures 1-3 are objected to under section 608.02(1) in the M.P.E.P. Portions of the figures are not consistent with the requirements as set forth in the aforementioned section, specifically with regards to "Every line, number, and letter must be...sufficiently dense and dark, and uniformly thick and well defined," Correction is required.

Applicant will provide drawing sheets for Figs. 1, 2, and 3 consistent with the MPEP when the application is allowed.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration allowance and passage to issue of the present application are respectfully requested.

35 USC §102 Rejections

The Examiner states:

Claims 1-3, 15, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohhata et al., U.S. 5,402,377.

As per claim 1:

Ohhata teaches of a secondary memory array that provides a cache for a memory unit (Fig. 2). Inclusive in the taught method of increasing the yield of the memory cell is a method of determining when an access is made to a failed memory bit location in the memory cell, and then substituting a memory location in the cached memory location when the defective location is accessed (Col. 2: 55-68).

As per claim 2:

Ohhata teaches of identifying each failed bit location and storing an indicati n f the failed mem ry bit location in the cache memory cell (Col. 2: 60-69).

As per claim 3:

The cached memory array of Ohhata acts as a lookup table (Fig. 2).

As per claim 15:

Claim 15 is the corresponding apparatus claim to method claim 1. As such, analogous reasoning can be used in the rejection of claim 15 as was used in the rejection of claim 1 above.

As per claim 18:

Claim 18 is the corresponding apparatus claim to method claim 2. As such, analogous reasoning can be used in the rejection of claim 18 as was used in the rejection of claim 2 above.

35 USC §103 Rejections

The Examiner states:

Claims 4, 6-7, 16-17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Bhavsar et al., U.S. 6,408,401.

As per claim 4:

Not explicitly taught by Ohhata is a method utilizing a comparison of the failed bit locations. Bhavsar teaches to a bit failure location comparison used for the purpose of identification of a faulty memory cell (Col. 2: 10-16). It would have been obvious for one of ordinary skill in the art at the time of the invention to made use of the comparison techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col. 2: 10-12).

As per claim 6:

The circuitry of Bhavsar allows for the cache to be of a SRAM type (Col. 2: 6-8).

As per claim 7:

The circuitry of Bhavsar allows for the cache t be f a DRAM type (Col. 2: 6-8).

As per claim 16:

Claim 16 is the corresponding apparatus claim to method claim 7. As such, analogous reasoning can be used in the rejection of claim 16 as was used in the rejection of claim 7 above.

As per claim 17:

Claim 17 is the corresponding apparatus claim to method claim 6. As such, analogous reasoning can be used in the rejection of claim 17 as was used in the rejection of claim 6 above.

As per claim 19:

Claim 19 is the corresponding apparatus claim to method claim 4. As such, analogous reasoning can be used in the rejection of claim 19 as was used in the rejection of claim 4 above.

Claims 5, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al. U.S. 5,402,377, in view of Douceur, U.S. 5,838,893.

As per claim 5:

Ohhata does not teach of a method including a pre-scan operation on the memory array for the purpose of identifying a failed memory cell location. Douceur teaches that it is known to make a determination of faulty memory cell locations upon device startup (Col. 1:47-56). It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col. 1: 55-56).

As per claim 8:

Shown above is a combination of Douceur and Ohhata that allows for a pre-scan operation to be performed whereby a memory location is swapped into a cache location.

As per claim 9:

The cache memory array f Ohhata is between a primary mem ry array, and a memory control unit (fig. 2).

As per claim 10:

The cached memory array of Ohhata acts as a lookup table (Fig. 2).

As per claim 11:

The memory control unit of Ohhata is responsible for the swapping of memory locations between the primary array and the cache memory array upon detection of a failed memory location (Col. 2: 55-69).

As per claim 12:

The memory control unit of Ohhata is responsible for the swapping of memory locations between the primary array and the cache memory array (Col. 2: 55-69).

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al. U.S. 5,402,377, in view of Douceur, U.S. 5,838,893, and in further view of Bhavsar et al., U.S. 6,408,401.

As per claim 13:

It has been shown above that it would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col. 1: 55-56). Likewise, it has been shown above that it too would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the comparison techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col 2: 10-12). Moreover, it was shown that the circuitry of Bhavsar allows for the cache to be of a DRAM type (Col. 2: 6-8). The combinations of the methods demonstrated above would have been obvious for one of ordinary skill in the art to make at the time of the invention because these combinations allow for early error location determinations to be made on the error status of the memory cell location, wherein the precision of the memory cell error notification becomes more precise, thus leading to better overall system functionaility.

As per claim 14:

It has been shown above that it w uld have been bvi us for ne f ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col. 1: 55-56). Likewise, it has been shown above that it too would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the comparison techniques taught by Bhavsar in conjunction with the method of Ohhata because the explicit comparison methodology allows for precise notification of faulty memory cells (Bhavsar, Col. 2: 10-12). Moreover, it was shown that the circuitry of Bhavsar allows for the cache to be of a SRAM type (Col. 2: 6-8). The combinations of the methods demonstrated above would have been obvious for one of ordinary skill in the art to make at the time of the invention because these combinations allow for early error location determinations to be made on the error status of the memory cell location, wherein the precision of the memory cell error notification becomes more precise, thus leading to better overall system functionality.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Bhavsar et al., U.S. 6,408,401, and Torrance et al. "A 33 GB/s 13.4 Mb Integrated Graphics Accelerator and Frame Buffer," IEEE International Solid-State Circuits Conference 1998.

As per claim 20:

Ohhata teaches of a secondary memory array that provides a cache for a memory unit (Fig. 2). Inclusive in the taught system for increasing the yield of the memory cell is a means for determining when an access is made to a failed memory bit location in the memory cell, and then substituting a memory location in the cached memory location when the defective location is accessed (Col. 2: 55-68). The circuitry of Bhavsar allows for the cache to be of a DRAM type (Col. 2: 6-8). Moreover, Torrance teaches that a system with a memory module can be utilized in conjunction with a graphics accelerator (Fig. 2). Therefore, it would have been obvious for one of ordinary skill in the art to combine graphic accelerator circuitry into the device of Ohhata, as adjusted above in the combination with Bhavsar, because Ohhata allows for the test mapping of the memory array circuit, a testing methodology which is cited as by Torrance as a means for testing the embedded memory cell of a graphics accelerator.

Applicant respectfully traverses these rejections. Claims 1, 8 and 15 are reproduced in their entirety hereinbelow.

Independent Claims

1. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

providing a cache for a memory unit;

determining when an access is made to a failed bit memory location in the memory unit, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table; and

substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed.

8. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

performing a memory pre-scan operation on an embedded memory device to identify each failed bit location in the embedded memory device;

storing each failed bit location in a look-up table; and

swapping a memory location within a cache for a failed bit location.

15. An embedded memory device with increased yield of usable memory locations, the embedded memory device comprising:

a memory unit;

a cache coupled to the memory unit; and

a memory control unit coupled to the memory unit and the cache, the memory control unit determining when an access is made to a failed bit memory location in the memory unit, and substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table.

Present Invention

The present invention meets this need and provides aspects for increasing yield in an embedded memory device. With the aspects of the present invention, a cache is provided for a memory unit of an embedded memory device. Attempts to access a failed

bit memory location in the memory unit are determined. When a failed memory bit location is being accessed, substitution of a memory location in the cache for the failed bit memory location occurs via a look-up table.

With the present invention, an efficient approach to increasing embedded memory device yield is provided. The provision of a cache to substitute for failed memory locations in a memory portion of the embedded memory device allows utilization of memory space substantially equivalent to the intended size of the memory portion. In this manner, the number of usable memory bit locations or yield of the memory portion is increased over prior art approaches of memory re-mapping. Further, the ability to maintain utilization of an embedded memory device with failed bit locations increases production yield, since fewer devices would need to be discarded. These and other advantages of the present invention will be more fully understood in a conjunction with the following detailed description and accompanying drawings.

ARGUMENTS

Neither Ohhata nor Bhavsar singly or in combination teach or suggest storing each failed bit location in a look-up table as recited in all of the independent claims. The Examiner has stated that the cached memory array of Ohhata acts as a look-up table as per Figure 2. Applicant nowhere within the reference can find such a description. The auxiliary memory cell array of Ohhata is accessed when an area in the primary cell array is defective. There is no teaching or suggestion of a look-up table. For the above-mentioned reasons the independent claims are allowable over the cited references.

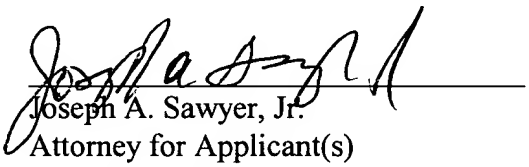
Moreover dependent claims 4-7, 9-14 and 16- 20 are allowable since they depend from an allowable base claim.

Applicant respectfully requests reconsideration and allowance of claims 1 and 4-20 as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP

December 9, 2003
Date



Joseph A. Sawyer, Jr.
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540